Shinnung Jeong

Curriculum Vitae

Contact Information

College of Computing, Georgia Institute of Technology
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Education

Yonsei University, Seoul, Republic of Korea
Integrate M.S./Ph.D. Student, March 2019 to February 2025
Advisor: Prof. Hanjun Kim

Pohang University of Science and Technology (POSTECH), Pohang, Republic of Korea
Bachelor of Science in Creative IT Engineering, March 2015 to February 2019

Experience

Postdoctoral Researcher, March 2025 to Present
High Performance Architecture Lab (HPArch), *Georgia Institute of Technology*, Atlanta, Georgia, USA

- Superviser: Prof. Haesun Park and Prof. Hyesoon Kim
- Design compiler and microarchitecture of the Open Source GPU, Vortex GPU.
- Design compiler and runtime for Numerical Linear Algebra.

Research Assistant, March 2019 to February 2025
Compiler Research Laboratory (Corelab), *Younsei University*, Seoul, Republic of Korea

- Design graph processing interface to enlarge design space for GPU (PACT'22)
- Develop locality-aware graph topology layout for GPU (ICPP'24)
- Develop thread-aware area optimized high-level synthesis framework for IoT devices (CGO'21)
- Design dynamic neural networks for real-time systems (ECRTS'22)
- Develop ML compiler based on MLIR framework for Samsung NPU (DAC'23)

Visiting Scholar, March 2023 to March 2024
High Performance Architecture Lab(HPArch), *Georgia Institute of Technology*, Atlanta, Georgia, USA

- Advisor: Prof. Hyesoon Kim
- Develop compiler of the Open Source GPU, Vortex GPU
- Expand the application support of the Vortex GPU (HPCA'25)

Undergraduate Research Assistant, December 2017 to June 2018
Compiler Research Laboratory (Corelab), *POSTECH*, Pohang, Republic of Korea

Undergraduate Research Assistant, June to August 2016, January to February 2017
POSTECH Database and Data Mining Lab (Big data lab), *POSTECH*, Pohang, Republic of Korea

Undergraduate Student Intern, September to December 2016
Excem, Pohang, Republic of Korea

Exchange Student, September 2015 to December 2015
University of California, Berkeley, United States of America

Recognition

- Magna Cum Laude from POSTECH, February 2019
- Excellence Award, Creative IT Design Competition, Department of Creative IT Engineering, POSTECH, June 2018
- PJ Metal Best Papers, Department of Humanities and social sciences, POSTECH, December 2018
- Excellence Award, 2018 POSTECH Hackathon Catch, PoApper, November 2018
- Excellence Award, Arthackathon : Next-generation culture and arts education with 4th Industrial Revolution Technology, Jun 2018
- The Grand Prize, Create IT Design Competition, Department of Creative IT Engineering, POSTECH, June 2016
- Vadas Award, Create IT Design Competition, Department of Creative IT Engineering, POSTECH, December 2016 (Award given to the most commercially successful project)
- Vadas Award, Create IT Design Competition, Department of Creative IT Engineering, POSTECH, June 2016

Activities

International Conference Reviewer

- Reviewer, Transactions on Architecture and Code Optimization (TACO), 2023

International Conference Sub-reviewer

- Sub-reviewer, The ACM/IEEE International Symposium on Code Generation and Optimization (CGO), 2022, 2021, 2020
- Sub-reviewer, IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), 2022, 2021
- Sub-reviewer, The 25th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2020
- Sub-reviewer, 2019 IEEE Micro, 2019

Invited Talks

- "Decoupling Schedule and Storage Format for Balanced Graph Processing on a GPU" presented at KYUNG HEE UNIVERSITY, June 23th, 2025.

Teaching

- EEE3313-01: Basic Digital Experiments, Yonsei University
  Teaching Assistant, Spring 2021 / Fall 2020 / Spring 2019
  (Teaching weekly lab classes about how to writing RTL Verilog code and designing hardware acceleration(FPGA-ARM))
- EEE3540-01: Microprocessor, Yonsei University
  Teaching Assistant, Fall 2019
  (Teaching weekly lab classes about programming related to microprocessor)

Publications

Refereed Journal Publications

[1] Bongjun Kim, Seonyeong Heo, Jaeho Lee, Shinnung Jeong, Yongwoo Lee, and Hanjun Kim, "Compiler-assisted Semantic-aware Encryption for Efficient and Secure Serverless Computing," in *IEEE Internet of Things Journal*, April 2021.
IF=9.936, Q1 (JCR 2019)

Refereed Conference Publications

[2] Shinnung Jeong, Liam Paul Cooper, Ju Min Lee, Heelim Choi, Nicholas Parnenzini, Chihyo Ahn, Yongwoo Lee, Hanjun Kim, and Hyesoon Kim, "SparseWeaver: Converting Sparse Operations as Dense Operations on GPUs for Graph Workloads," in *2025 IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, March 2025.

[3] Shinnung Jeong and Hanjun Kim, "Matrix Pattern-aware Partitioning and Auto-tuning Space Pruning for Graph Processing on GPU," in *The 9th International Conference On Consumer Electronics Asia (ICCE-ASIA)*, November 2024.

[4] Shinnung Jeong, Sungjun Cho, Yongwoo Lee, Hyunjun Park, Seonyeong Heo, Gwangsun Kim, Youngsok Kim, and Hanjun Kim, "CR2: Community-aware Compressed Regular Representation for Graph Processing on a GPU," in *Proceedings of the 53rd International Conference on Parallel Processing (ICPP)*, August 2024.

[5] Seungbin Song, Ju Min Lee, Haeeun Jeong, Hyunho Kwon, Shinnung Jeong, Jaeho Lee, and Hanjun Kim, "TeMCO: Tensor Memory Compiler Optimization across Tensor Decompositions in Deep Learning Inference," in *Proceedings of the 53rd International Conference on Parallel Processing (ICPP)*, August 2024.

[6] Jaeho Lee, Shinnung Jeong, Seungbin Song, Kunwoo Kim, Heelim Choi, Youngsok Kim, and Hanjun Kim, "Occamy: Memory-efficient GPU Compiler for DNN Inference," in *Proceedings of the 60th Annual Design Automation Conference 2023 (DAC)*, July 2023.

[7] Shinnung Jeong, Yongwoo Lee, Jaeho Lee, Heelim Choi, Seungbin Song, Jinho Lee, Youngsok Kim, and Hanjun Kim, "Decoupling Schedule, Topology Layout, and Algorithm to Easily Enlarge the Tuning Space of GPU Graph Processing," in *Proceedings of the 31st International Conference on Parallel Architectures and Compilation Techniques (PACT)*, October 2022.

[8] Seonyeong Heo, Shinnung Jeong, and Hanjun Kim, "RTScale: Sensitivity-Aware Adaptive Image Scaling for Real-Time Object Detection," in *34th Euromicro Conference on Real-Time Systems (ECRTS)*, July 2022.

[9] Yongwoo Lee, Seonyeong Heo, Seonyoung Cheon, Shinnung Jeong, Changsu Kim, Eunkyung Kim, Dongyoon Lee, and Hanjun Kim, "HECATE: Performance-Aware Scale Optimization for Homomorphic Encryption Compiler," in *Proceedings of the 2022 International Symposium on Code Generation and Optimization (CGO)*, April 2022.

[10] Changsu Kim, Shinnung Jeong, Sungjun Cho, Yongwoo Lee, William Song, Youngsok Kim, and Hanjun Kim, "Thread-Aware Area-Efficient High-Level Synthesis Compiler for Embedded Devices," in *Proceedings of the 2021 International Symposium on Code Generation and Optimization (CGO)*, March 2021.

Refereed Workshop Publications

[11] Huanzhi Pu, Rishabh Ravi, Shinnung Jeong, Udit Subramanya, Euijun Chung, Jisheng Zhao, Chihyo Ahn, and Hyesoon Kim, "Hardware vs. Software Implementation of Warp-Level Features in Vortex RISC-V GPU ," in *Open Source Solutions for Massively Parallel Integrated Circuits (OSSMPIC)*, April 2025.

[12] Chihyo Ahn, Shinnung Jeong, Liam Paul Cooper, Nicholas Parnenzini, and Hyesoon Kim, "Comparative Analysis of Executing GPU Applications on FPGA: HLS vs. Soft GPU Approaches ," in *The Third International Workshop on Coarse-Grained Reconfigurable Architectures for High-Performance Computing (CGRA)*, May 2024.

Refereed Poster Publications

[13] Chan Lee, Shinnung Jeong, Heelim Choi, Jaeho Lee, Haeeun Jeong, Hoyun Youm, Ju Min Lee, and Hanjun Kim, "Approximation-based Inter-PE Communication-free Image Filtering for Commodity PIM," to appear in *Proceedings of the 62th Annual Design Automation Conference 2025 - (Poster) (DAC)*, June 2025.

[14] Changsu Kim, Yongwoo Lee, Shinnung Jeong, and Hanjun Kim, "Logic Deduplication with Decentralized Pointer Analysis in HLS for Post-Quantum Cryptography Algorithms," in *Proceedings of the 57th Annual Design Automation Conference 2020 - (Poster) (DAC)*, July 2020.

[15] Changsu Kim, Yongwoo Lee, Shinnung Jeong, Wen Wang, Jakub Szefer, and Hanjun Kim, "Pipeline-aware Logic Deduplication in High-Level Synthesis for Post-Quantum Cryptography Algorithms," in *Proceedings of the 2020 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, February 2020.

Other Publications

[16] Shinnung Jeong, "Decoupling Scheduling and Storage Formats for Balanced Graph Processing on a GPU," Ph.D. Dissertation, Yonsei University, February 2025.

Patents

[17] Hanjun Kim, Bongjun Kim, Jaeho Lee, Seonyeong Heo, Shinnung Jeong, and Yongwoo Lee, "IoT Service Providing Method Based on Adaptive Encryption and IoT Apparatus," KR Patent Number 10-2508448-0000, March 2024.

[18] Hanjun Kim, Youngsok Kim, Changsu Kim, Shinnung Jeong, Yongwoo Lee, Sungjun Cho, and William Song, "High-Level Synthesis Method and Apparatus for Hardware Optimization," KR Patent App. 10-2022-0023420, February 2022.